FPGA Digital Signal Processing

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DEREK KOZEL

- Electrical and Computer Engineering
- US Extra Licence - AG6PO
- Amateur Radio in University (W3VC, W6CMU)
- Radio at work
  - Distributed sensor networks
  - SDR Cellular basestations
  - General Purpose SDR (Ettus)
- Living in Cardiff, Wales, UK, Europe, Earth

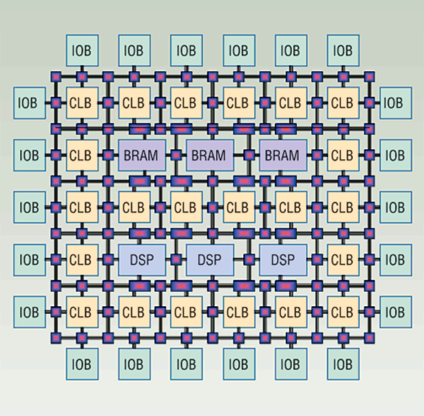
Field Programmable Gate Arrays (FPGAs)

WHAT ARE FPGAS

- Integrated Circuits containing a complex array of logic cells, memory, DSP units, and optional extra interfaces
- Logic operations can be reprogrammed repeatedly
- Slower than dedicated ICs, but flexible like software

ALTERA®

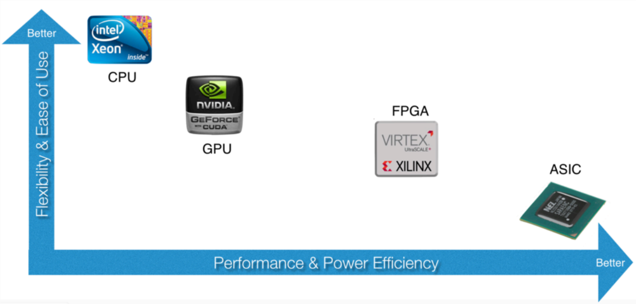
XILINX®



	IOB	IOB	IOB	IOB	IOB	IOB	
IOB	CLB	CLB	CLB	CLB	CLB	CLB	IOB
IOB	CLB	BRAM		BRAM	BRAM	CLB	IOB
IOB	CLB	CLB	CLB	CLB	CLB	CLB	IOB
IOB	CLB	DSP		DSP	DSP	CLB	IOB
IOB	CLB	CLB	CLB	CLB	CLB	CLB	IOB
	IOB	IOB	IOB	IOB	IOB	IOB	

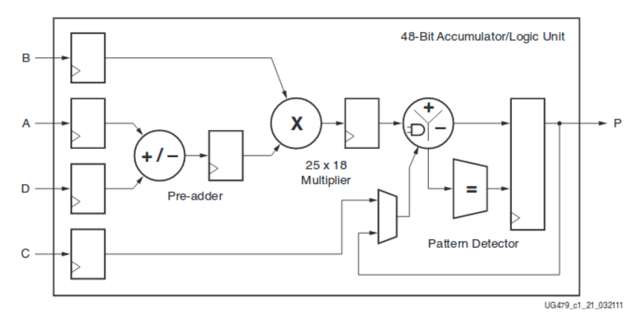
WHY USE FPGAS?

- Best of high bandwidth frontend, low datarate to host
- Can be energy efficient vs CPUs or GPUs
- Very good at realtime stream processing



FPGA INSIDES

- Logic resources are grouped into slices (Configurable Logic Blocks)
  - Look Up Tables (LUT)
  - Flip-Flips
  - Multiplexers (Muxes)
- Block RAM: configurable memory modules
- DSP Slice: add/subtract, multiply, accumulate, magic

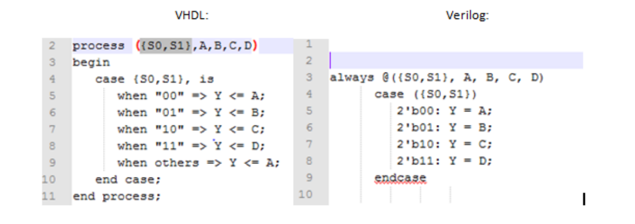


FPGA Programming Options

HARDWARE DESCRIPTION LANGUAGES

[fragile]

- (System)Verilog and VHDL
- PyHDL, SystemC, ...



VHDL:

```
process ({S0,S1},A,B,C,D)
begin
   case {S0,S1}, is
      when "00" => Y <= A;
      when "01" => Y <= B;
      when "10" => Y <= C;
      when "11" => Y <= D;
      when others => Y <= A;
   end case;
end process;
```

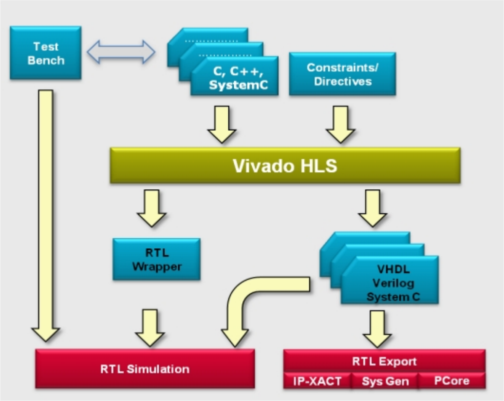
Verilog:

```


always @({S0,S1}, A, B, C, D)
   case ({S0,S1})
      2'b00: Y = A;
      2'b01: Y = B;
      2'b10: Y = C;
      2'b11: Y = D;
   endcase
```

XILINX HIGH LEVEL SYNTHESIS

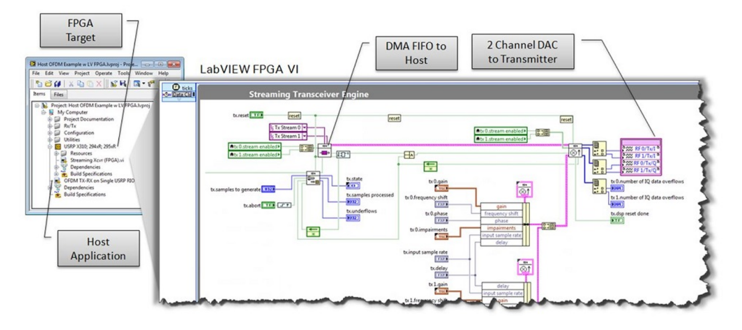
- ”Compile” C, C++, or SystemC to an FPGA bitstream



Source: Vivado Design Suite User Guide High-Level Synthesis UG902

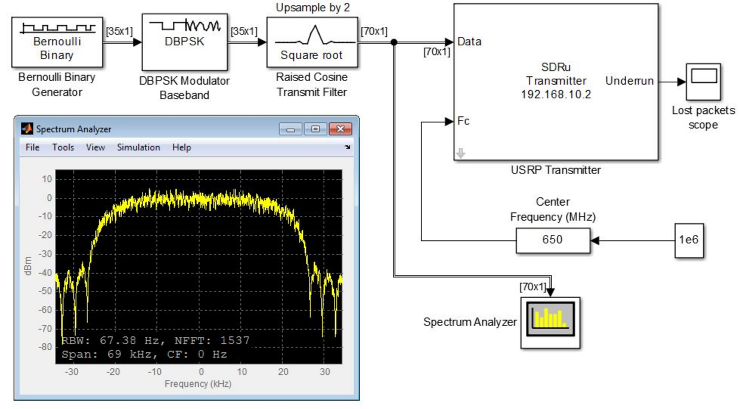
LABVIEW FPGA

- Graphical Block based library of IP
- Generates FPGA and host code



MATLAB SIMULINK

- Graphical environment with IP generators for a variety of DSP operations
- Can synthesize the FPGA image along with host code

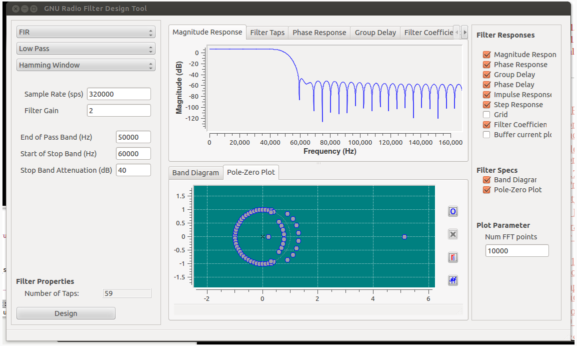


Common DSP Elements

EXAMPLE SDR TRANSCEIVER

FILTERS

- Finite Impulse Response (FIR) Filter
- Halfband Filter
  - Symmetrical coefficients allow for a 50% smaller filter



GNU Radio Filter Design Tool

FIR

Low Pass

Hamming Window

Sample Rate (sps): 320000

Filter Gain: 2

End of Pass Band (Hz): 50000

Start of Stop Band (Hz): 60000

Stop Band Attenuation (dB): 40

Filter Properties

Number of Taps: 59

Design

Filter Responses

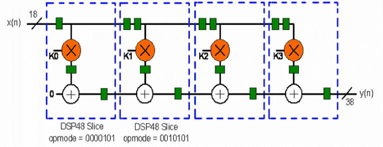
- ☑ Magnitude Respon
- ☑ Phase Response
- ☑ Group Delay
- ☑ Phase Delay
- ☑ Impulse Respons
- ☑ Step Response
- □ Grid
- ☑ Filter Coefficien
- □ Buffer current pl

Filter Specs

- ☑ Band Diagrar
- ☑ Pole-Zero Plot

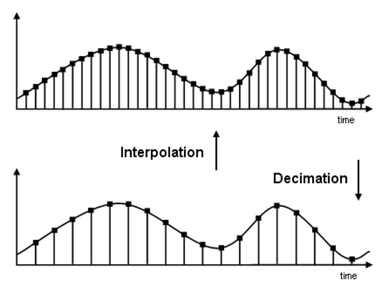
Plot Parameter

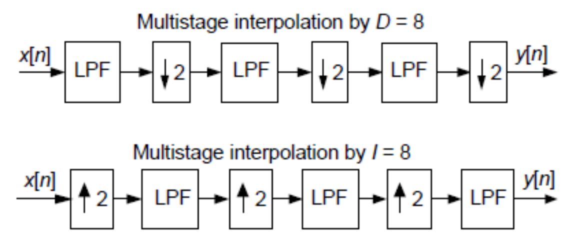
Num FFT points: 10000



RATE CHANGES

- Interpolation and Decimation
  - Reduces the sample rate the host must handle
  - Decimation can improve SNR

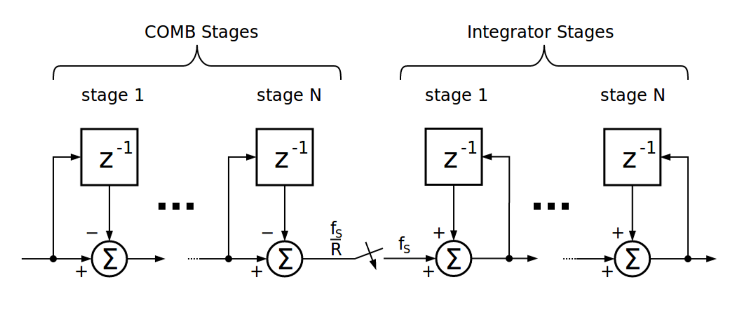



Multistage interpolation by D = 8
x[n]
LPF
↓2
LPF
↓2
LPF
↓2
y[n]
Multistage interpolation by I = 8
x[n]
↑2
LPF
↑2
LPF
↑2
LPF
y[n]

RATE CHANGES – CIC

Cascaded-Integrator-Comb Filter

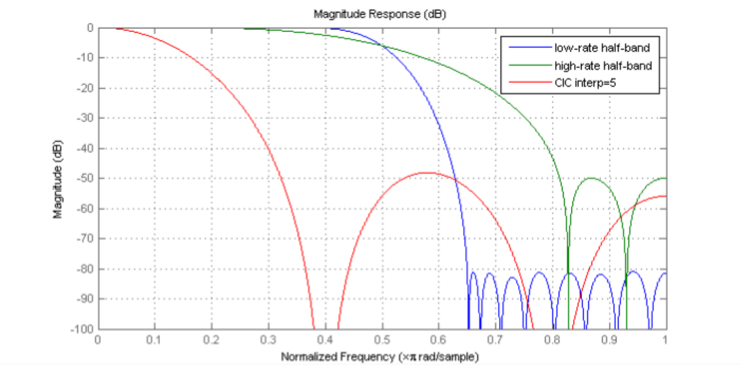
- Optimized FIR filter
- Allows for flexible decimation (ie divide by 1-255)
- Can work as a moving average as well



RATE CHANGES – CIC

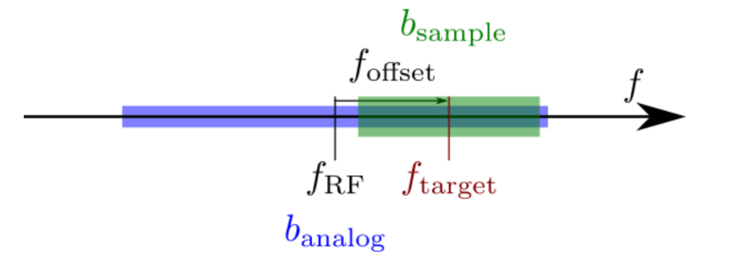
Cascaded-Integrator-Comb Filter

- Has poor filter roll off at odd rates
- A compensation filter can be added to reduce the impact



FREQUENCY SHIFTING

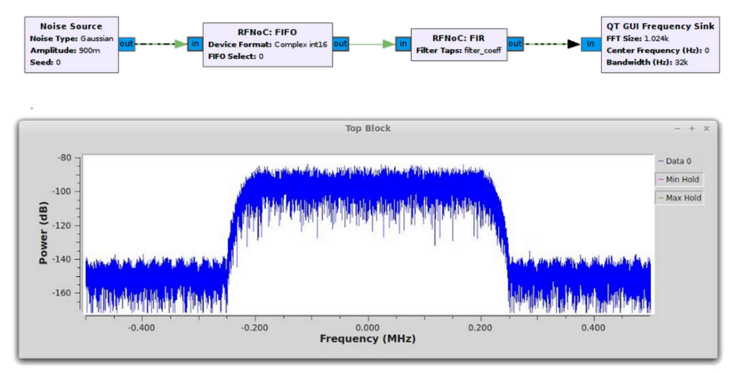
- CORDIC
- Quarter Rate Downconverter



RF Network on Chip

RFNOC

- FPGA data flow architecture to simplify DSP development and use
- Standard AXI interface for data processing
- Software API for register access
- Allows for runtime reconfiguration



Noise Source
Noise Type: Gaussian
Amplitude: 900m
Seed: 0

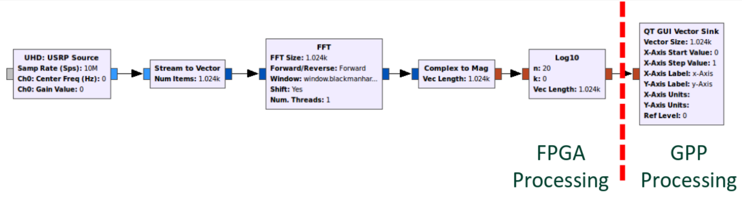
RFNoC: FIFO
Device Format: Complex int16
FIFO Select: 0

RFNoC: FIR
Filter Taps: filter_coeff

QT GUI Frequency Sink
FFT Size: 1.024k
Center Frequency (Hz): 0
Bandwidth (Hz): 32k

RFNOC

- Better to move computation into the FPGA
- CPU usage savings and a 50% datarate reduction to the host



UHD: USRP Source
Samp Rate (Sps): 10M
Ch0: Center Freq (Hz): 0
Ch0: Gain Value: 0

Stream to Vector
Num Items: 1.024k

FFT
FFT Size: 1.024k
Forward/Reverse: Forward
Window: window.blackmanhar...
Shift: Yes
Num. Threads: 1

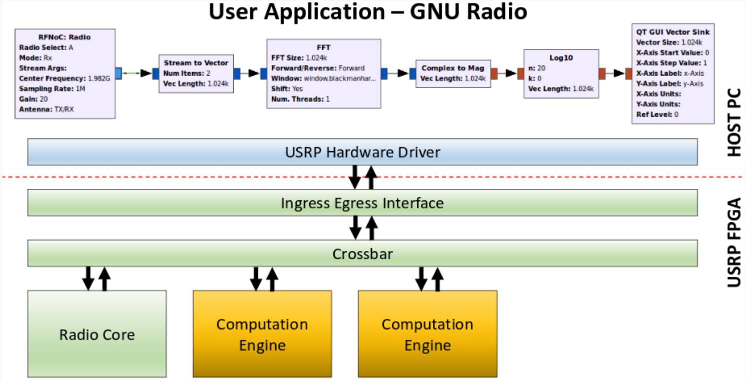
Complex to Mag
Vec Length: 1.024k

Log10
n: 20
k: 0
Vec Length: 1.024k

QT GUI Vector Sink
Vector Size: 1.024k
X-Axis Start Value: 0
X-Axis Step Value: 1
X-Axis Label: x-Axis
Y-Axis Label: y-Axis
X-Axis Units:
Y-Axis Units:
Ref Level: 0

RFNOC ARCHITECTURE

- Reconfigurable, flexible, ”simple” API
- Framework handles packetization, access to registers



User Application – GNU Radio

RFNoC: Radio
Radio Select: A
Mode: Rx
Stream Args:
Center Frequency: 1.982G
Sampling Rate: 1M
Gain: 20
Antenna: TX/RX

Stream to Vector
Num Items: 2
Vec Length: 1.024k

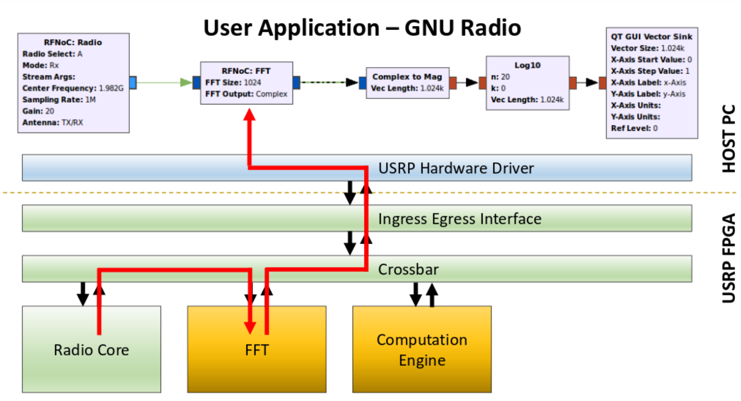
FFT
FFT Size: 1.024k
Forward/Reverse: Forward
Window: window.blackmanhar...
Shift: Yes
Num. Threads: 1

Complex to Mag
Vec Length: 1.024k

Log10
n: 20
k: 0
Vec Length: 1.024k

QT GUI Vector Sink
Vector Size: 1.024k
X-Axis Start Value: 0
X-Axis Step Value: 1
X-Axis Label: x-Axis
Y-Axis Label: y-Axis
X-Axis Units:
Y-Axis Units:
Ref Level: 0

RFNOC ARCHITECTURE



User Application – GNU Radio

RFNoC: Radio
Radio Select: A
Mode: Rx
Stream Args:
Center Frequency: 1.982G
Sampling Rate: 1M
Gain: 20
Antenna: TX/RX

RFNoC: FFT
FFT Size: 1024
FFT Output: Complex

Complex to Mag
Vec Length: 1.024k

Log10
n: 20
k: 0
Vec Length: 1.024k

QT GUI Vector Sink
Vector Size: 1.024k
X-Axis Start Value: 0
X-Axis Step Value: 1
X-Axis Label: x-Axis
Y-Axis Label: y-Axis
X-Axis Units:
Y-Axis Units:
Ref Level: 0

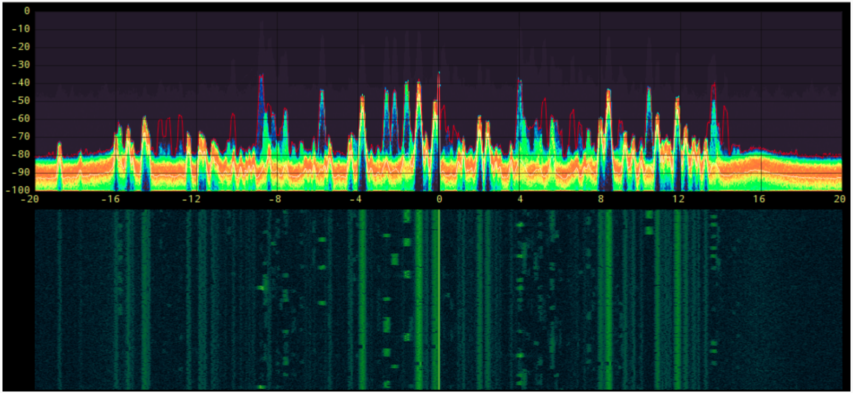
RFNOC BLOCKS

- A collection of Computation Engine blocks included in UHD and GNU Radio
- Some common blocks
    - Digital Down Converter, Digital Up Converter, FFT, FIR filter, Signal Generator, Vector IIR
- Basics
    - Digital Gain, Keep 1 in N, Log Power, Split Stream, DmaFIFO, Adder/Subtractor
- Modulation components
    - OFDM Sync, Equalizer, Constellation Demodulator

Applications

FOSPHOR

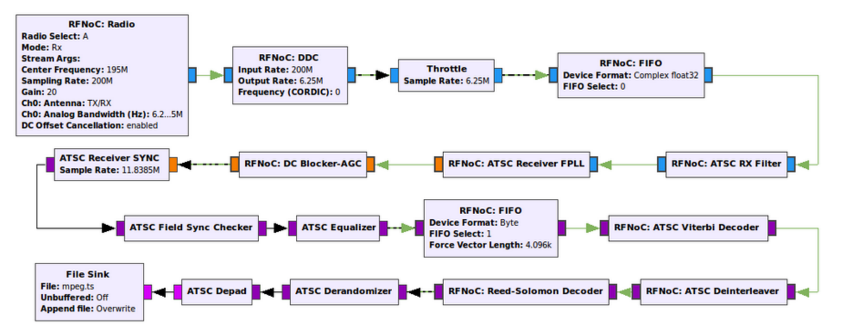
- Realtime Spectrum Analyzer application
- Developed by Sylvain Manaut
- FPGA calculates FFTs and heatmap
- Massively reduced throughput to host, minimal cpu load



- Sponsored by Ettus Research and Xilinx
- USD $10,000 prize, hardware prizes for runners up
- Many entries, three finalists

ATSC RECEPTION

- Demodulating digital television in the FPGA
- Developed by:
  - Andrew Valenzuela Lanez | andrew.lanez@navy.mil
  - Sachin Bharadwaj Sundramurthy | sbharad@eng.ucsd.edu
  - Alireza Khodamoradi | alirezak@eng.ucsd.edu



RFNoC: Radio
Radio Select: A
Mode: Rx
Stream Args:
Center Frequency: 195M
Sampling Rate: 200M
Gain: 20
Ch0: Antenna: TX/RX
Ch0: Analog Bandwidth (Hz): 6.2...5M
DC Offset Cancellation: enabled

RFNoC: DDC
Input Rate: 200M
Output Rate: 6.25M
Frequency (CORDIC): 0

Throttle
Sample Rate: 6.25M

RFNoC: FIFO
Device Format: Complex float32
FIFO Select: 0

RFNoC: ATSC RX Filter

RFNoC: ATSC Receiver FPLL

RFNoC: DC Blocker-AGC

ATSC Receiver SYNC
Sample Rate: 11.8385M

ATSC Field Sync Checker

ATSC Equalizer

RFNoC: FIFO
Device Format: Byte
FIFO Select: 1
Force Vector Length: 4.096k

RFNoC: ATSC Viterbi Decoder

RFNoC: ATSC Deinterleaver

RFNoC: Reed-Solomon Decoder

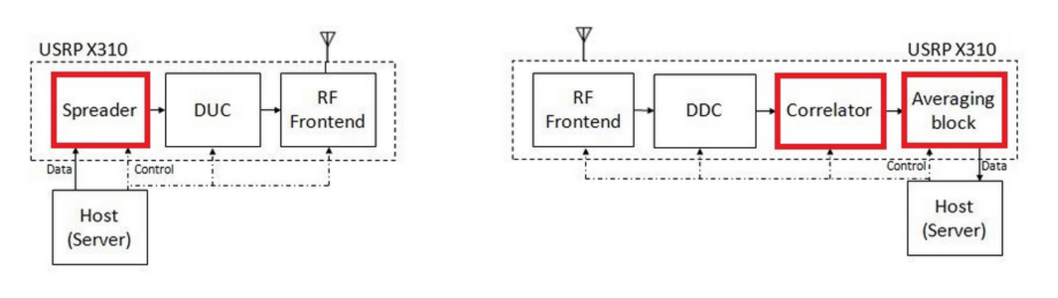
ATSC Derandomizer

ATSC Depad

File Sink
File: mpeg.ts
Unbuffered: Off
Append file: Overwrite

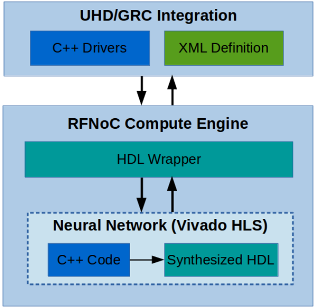
WIDE BAND CHANNEL SOUNDER

- Characterizing the properties of an RF link
- Developed by:
  - Bhargav Gokalgandhi bvg8@scarletmail.rutgers.edu
  - Prasanthi Maddala prasanti@winlab.rutgers.edu
  - Ivan Seskar seskar@winlab.rutgers.edu



NEURAL NETWORKS

- Neural Network based DSP
- Developed by:
  - EJ Kreinar ejkreinar@gmail.com


UHD/GRC Integration

C++ Drivers

XML Definition

RFNoC Compute Engine

HDL Wrapper

Neural Network (Vivado HLS)

C++ Code

Synthesized HDL

QUESTIONS

Questions?

The latest version of these slides can always be found at
`http://www.derekkozel.com/talks`

@derekkozel

GNU RADIO CONFERENCE

GNU Radio Conference is being held in San Diego in September!

`http://www.gnuradio.org`

AMSAT PHASE 4B

AMSAT's Phase 4B satellite and groundstation will likely use FPGA based SDRs!

`https://phase4ground.github.io/`

COLOPHON

The presentation was created using XeTeX and Beamer using the Metropolis theme.

`github.com/matze/mtheme`